REMARKS

In the office action mailed on December 28, 2005, claims 1 - 5, 8 - 12 and 14 - 19 were rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,724,003 (to Jensen et al.) and claims 6 and 7 were rejected under 35 U.S.C. §103(a) over the Jensen et al. reference in view of U.S. Patent No. 6,348,781 (to Midya et al.).

The Jensen et al. reference discloses, in part, a linearized power sensor circuit that includes a power sampling circuit 408, a variable gain amplifier (VGA) 412, a power detector 418 and an error amplifier circuit 424 as shown in Figures 4 and 6. The power sensor circuit is disclosed to provide highly linearized power detection (Jensen et al., col.10, lines 43 - 45). The linearized power sensor circuit of Figure 6 is also disclosed to include a first feedback path from the output of the error amplifier circuit 424 to a control input of the VGA 412. The circuit of Figure 6 also includes a second feedback path that includes an analog-to-digital converter (ADC) 512 that provides a feedback signal to a microcontroller 514. The microcontroller 514 provides the control signal 516 to the RF power amplifier 402, which provides the amplitude controlled signal 404.

The Jensen et al. reference, however, does not disclose that the VGA 412 includes any transfer function ripple either with or without feedback. If the VGA 412 does include a transfer function ripple, the capacitor C1 in the error amplifier circuit 424 would be known to be relatively large (to ensure proper control of the dynamic range of the error amplifier) that any noise at the output of the detector 418 would be removed by the error amplifier.

In particular, neither the feedback path to the VGA 412 nor the feedback path to the ADC 512 would act to reduce any transfer function ripple. The feedback path from the error amplifier

424 to the VGA 412 is used to either amplify or attenuate the sensed signal on line 410 to ensure that the power detector 418 operates in a linear fashion over the entire dynamic range of the wide dynamic range amplitude-controlled signal on line 404 (Jensen et al., col.5, lines 32-49; col.6, lines 28-37; and col.10, lines 24-27). This feedback path, therefore, shifts the operating range of the VGA 412 so that the input to the error amplifier remains in a linear range.

Applicant submit, therefore, that any transfer function ripple of the VGA 412 (which is not disclosed to exist in Jensen et al.) would not be removed by the feedback path from the error amplifier 424 to the control input of the 412 because the control input is employed to ensure that the power detector 418 operates over the entire dynamic range of the amplitude-controlled signal 404.

The feedback path to the microcontroller 514 that includes the ADC 512 would also not act to reduce any transfer function ripple because this digital feedback path to the microcontroller 514 is disclosed to be used to adjust the output power level of the RF power amplifier 402 to achieve a desired output power level of the power amplifier 402. Not only is this feedback not provided to the VGA 412, but it is disclosed to provide linear control of the output of the power amplifier 402, not a reduction in transfer function ripple.

The Midya et al. reference discloses a converter system in which a buck converter is cascaded with a boost converter. The converter system appears to be controlled by a controller such that only the buck or boost converter is operating at any given time. A reference signal is disclosed to be applied to the controller such that the output voltage from the converter closely tracks the reference signal. The Midya et al. reference also does not disclose the use of any feedback path to reduce transfer function ripple of a VGA.

Claim 1 is directed to an RMS-to-DC converter that includes, in part, a variable gain

amplifier having transfer function ripple, and a feedback control circuit that provides a feedback signal to the variable gain amplifier that includes an AC component for reducing transfer function ripple of the RMS-to-DC converter. Neither the Jensen et al. nor the Midya et al. reference in any combination discloses such a system as claimed in claim 1. Claim 1, therefore, is submitted to be in condition for allowance. Each of claims 2 - 11 depends directly or indirectly from claim 1 and is also submitted to be in condition for allowance.

Claim 12 is also directed to an RMS-to-DC converter that includes, in part, a variable gain amplifier having transfer function ripple, and a feedback control circuit that provides a feedback signal to the variable gain amplifier that includes an AC component for reducing transfer function ripple of the RMS-to-DC converter. Neither the Jensen et al. nor the Midya et al. reference in any combination discloses such a system as claimed in claim 12. Claim 12, therefore, is submitted to be in condition for allowance. Each of claims 13 - 16 depends directly or indirectly from claim 12 and is also submitted to be in condition for allowance.

Claim 17 is directed to a method of providing an RMS-to-DC conversion that includes, in part, the steps of receiving an input signal and providing an amplifier output signal by a variable gain amplifier having a transfer function ripple, and coupling the error amplifier output signal to the variable gain amplifier for providing a feedback signal to the variable gain amplifier that includes an AC component for reducing transfer function ripple of the RMS-to-DC converter system. Neither the Jensen et al. nor the Midya et al. reference in any combination discloses such a system as claimed in claim 17. Claim 17, therefore, is submitted to be in condition for allowance. Each of claims 18 and 19 depends directly or indirectly from claim 17 and is also submitted to be in condition for allowance.

Each of claims 1 - 19, therefore, is considered to be in condition for allowance.

Favorable action consistent with the above is respectfully requested.

Respectfully submitted,

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